OISTO
SUPER PRODUCTS

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THE SUPER CONTROLLER II

PRINTED IN CANADA

DISTO

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INSTRUCTION MANUAL

Introduction

Congratulations, you have just bought one of the finest Color Computer disk controllers available today. The **DISTO Super Controller II** or better known as the **SC II**, employs the latest state-of-the-art technology for floppy disk controllers, the Western Digital WD1773. Also, the premium-quality, solid-state circuitry assures high reliability for your personal or business use. This controller is upward compatible to the Radio Shack Color Computer disk controller. This means that it will do everything the Radio Shack controller can and more.

Features:

- **Radio Shack / Tandy compatible.**
- **Works on all COCOs 1, 2 or 3 with or without the Multi-Pak Interface.**
- **One 24/28 pin socket, for 8K ROM, 2764, 27128 or 27256.**
- **Internal Mini-Expansion-Bus Connector for one DISTO Super Adapter Add-on.**
- **Low Power Draw; Within COCO's power requirements.**
- **All Gold Plated edge connectors.**
- **Under OS-9:**
  - Buffered Read/Write sector is achieved without halting the CPU.
  - Continual use of keyboard even while Reading/Writing to disk.
  - System Clock no longer looses time during Read/Write.
  - NMI is blocked and transferred to IRQ in software for low CPU overhead.
  - Completely interrupt driven for Fast & Smooth Multi-Tasking operations.
  - Drivers for Level 1 (2.XX only) & Level 2 are written by Keven Darling. (Included).

Description:

This controller has two modes of operation. The first is the Normal mode. This is the default mode on power-up. This mode is compatible with the **Super Controller I** and the Radio Shack/Tandy controller. The second is the Buffered mode. With the proper driver software, in this mode, all sectors being written to or read from the diskette will be done via a sector buffer. A sector buffer is a separate circuit inside the **SC II** that has its own RAM. In the normal mode, when the CPU reads or writes a sector, it has to give the FDC (Floppy Disk Controller) the command, and wait for the FDC to locate the sector. It then has to assist, the FDC to transfer the data to and from the disk and its own memory, waiting for each byte to go by. This is relatively slow and all this time, the CPU cannot do anything else because it is halted between bytes.

The Buffered mode is different. The CPU gives the FDC its command and then switches the **SC II** to the Buffered mode. At this time, the CPU is free to do other things while the Buffer circuitry takes over the task of waiting for the FDC, and transferring the data to and from the on-board RAM. After this task is finished, the FDC then signals the CPU that the operation is finished, at which point, the CPU can read the data from the on-board buffer (RAM) or load it up for another operation.

The **SC II** also has a MEB bus, which is a 17 pin internal expansion bus. Its main use is for our optional **Real-Time Clock and Centronics Compatible Parallel Printer adapter add-on**. Other options such as a low-cost **EPROM Programmer** or a **Hard disk adapter** are also available.

Memory Map (I/O control):

Though this controller's memory map is compatible with the Radio Shack controller, it is somewhat modified to accommodate the extra features. Table 1 is a memory map of the ($\overline{SCS}$) select pin of the Color Computer as used by this controller. This I/O select is mapped at $FF40 (65344) to $FF5F (65375). The SC II also requires 4 address locations for its control and data registers. These 4 locations have been assigned to **DISTO** by Tandy. They are from $FF74 (65396) to $FF77 (65399) inclusive. Table 2 shows the use of these 4 address locations. In some cases, these address locations may interfere with other hardware devices connected to your computer. The **SC II** has an alternate location for its control and data registers. They are located in the ($\overline{SCS}$) memory map, see Table 1. To change the memory map from the normal area to the alternate area, change the jumper J3 from (1 & 2) to (2 & 3). See Figure 1 for the location of J3.

Table 1
($\overline{SCS}$) Memory Map

Location Hex	Location Decimal	Description SC II	Description Radio Shack
FF40	65344	Drive Selector	Drive Selector
FF41 to FF47	65345 to 65351	Mirror of FF40	Mirror of FF40
FF48	65352	FDC Status Reg	FDC Status Reg
FF49	65353	FDC Track Reg	FDC Track Reg
FF4A	65354	FDC Sector Reg	FDC Sector Reg
FF4B	65355	FDC Data Reg	FDC Data Reg
FF4C to FF4F	65356 to 65359	Mirror of FF48 to FF4B	Mirror of FF48 to FF4B
FF50 to FF57	65360 to 65367	Mini-Expansion-Bus Memory Location	Mirror of FF48 to FF4B
FF58 to FF5F	65368 to 65375	Alternate to **SC II** control Registers	Mirror of FF48 to FF4B

Table 2
SC II Registers

Location Hex	Location Decimal	Description
FF74	65396	Write D0 = 0 FDC Write Operation *1 = 1 FDC Read Operation *1 D1 = 0 Normal Mode = 1 Buffered I/O Mode D2 = 0 Normal NMI = 1 Masked NMI D3 = 0 No FIRQ (Masked) = 1 Enabled FIRQ Read D7 = FDC INT Status (Inverted)
FF75	65387	Mirror of FF74 (65396)
FF76	65398	Read/Write Buffer Data *2
FF77	65399	Mirror of FF75 (65387) (Allows STD or LDD, any mode)

*1: In buffered mode only
*2: Any Write to $FF74 or $FF75 clears Buffer counter.

Memory Map of ($\overline{CTS}$):

The ($\overline{CTS}$) memory map area is from $C000 to $FEFF for the COCO 1 & 2 and from $C000 to $FDFF for the COCO 3. Under normal operations, this area contains a DOS chip. This can be a straight Radio Shack DOS or any other DOS that fits in a 24 pin ROM or EPROM, or any 2764, 27128, 27256. (A small modification is needed to access all of the 27256). There are three jumpers on the right side of the 28 pin socket. These jumpers determine what chip can be inserted into this socket. For a 24 pin ROM, set the jumper as follows: J4 - 1 & 2, J5 - 1 & 2, and J6 -1 & 2. The ROM should then be installed starting on pin 3 of the socket, leaving pins 1, 2, 27 and 28 free. For any other EPROM, set the jumpers as follows: J4 -2 & 3, J5 - 2 & 3, J6 - 2 & 3. See Figure 1 for proper location of J4, J5 and J6.

Mini-Expansion Bus:

J1 is the internal Mini-Expansion Bus. It consist of a 17 pin Single In-line Header. Figure 1 shows the location of the Mini-Expansion Bus. I call it a "Mini" because it includes only 8 memory locations. It is memory-mapped from $FF50 (65360) to $FF57 (65367). This area of memory is normally not available using a regular controller, due to memory mirroring of other functions. The **DISTO Super Controller**, however, properly decodes this area, therefore leaving a small area open for the Mini-Expansion Bus. Table 3 details the pinout of this Expansion bus. Any peripheral device needing 8 address locations or less can be attached to the Mini-Expansion Bus. J2 on the **SC II** is connected to the FIRQ of the COCO. Any device needing the FIRQ may be connected to J2.

Table 3
Mini-Expansion Bus Pinout.

Pin number:	Function
1	RESET
2	E CLOCK
3	Address 0
4	Address 1
5	Data 0
6	Data 1
7	Data 2
8	Data 3
9	Data 4
10	Data 5
11	Data 6
12	Data 7
13	Chip Enable ($\overline{CE}$)
14	GND
15	R/W
16	+ 5V
17	Address 2

Installation:

The **DISTO Super Controller** is very simple to install, however, if you follow these few rules, you will prevent any accident that you might be sorry for later. **Never, I said NEVER, plug or unplug the controller when the power is on.** Always turn the disk drive off before connecting or disconnecting the drive cable. When you take the cover off to change DOSes or to add-in an option, make sure that you and the controller are grounded. Static electricity can damage the components inside the controller. When replacing the lid, do not over-tighten the screws. If the edge contacts get dirty, clean them with a swab and a little lighter fluid.

Credits:

The DISTO Super Controller II, add-ons and all its documentation are conceived and designed by **Tony DIStefano**. The **DISTO Super Controller II** and **Add-ons** are manufactured and distributed by:

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Figure 1
Component layout